UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,792	12/03/2003	Srikanth T. Srinivasan	42P17888	6794

8791 · 7590 07/16/2007
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ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
07/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>09 April 2007</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16 and 18-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16 and 18-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1, 3-16, and 18-30 have been examined.

2.   It is hereby acknowledged that the following papers have been received and

placed of record in the file: Amendment as received on 04/09/2007.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 1, 3-16, and 18-30 are rejected under 35 U.S.C. 112, first paragraph, as

failing to comply with the enablement requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to enable one skilled in

the art to which it pertains, or with which it is most nearly connected, to make and/or use

the invention. More specifically, independent claims 1, 10, 16, and 25 recite limitations

indicating that (using claim 1 as exemplary) "said scheduler to re-execute selected

instructions of said program subsequent to said branch point, only upon detecting said

exact convergence point" [emphasis added]. This limitation indicates that only upon

detecting an exact convergence point (as defined earlier in the claims) does the

scheduler re-execute selected instructions of the program subsequent to a branch point.

As recognized by one of ordinary skill in the art, whenever there is a branch

misprediction (whether or not an exact convergence point is detected), instructions that

are control independent and data dependent must be re-executed. The reason for this

requirement is that in order to maintain integrity of a program, all instructions on the

correct path must be executed using the correct data dependencies. However, the

above-cited limitation indicates that in instances where control independent and data

dependent instructions must be re-executed (in order to maintain program integrity),

they are not re-executed since an exact convergence point was not detected. Since the

applicant's specification does not describe how program integrity is maintained in these

instances, the examiner has found no support in the specification for the above-cited

limitation (and similar limitations in the other independent claims). Therefore, the

applicant's specification does not enable one skilled in the art to make and use the

invention.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1, 3-5, 8-14, 16, 18-20, and 23-29 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Chou et al., "Reducing Branch Misprediction Penalties Via

Dynamic Control Independence Detection", (Herein referred to as Chou) in view of

Keller et al., U.S. Patent No. 6,542,984, (Herein referred to as Keller).

7.   Referring to claim 1, Chou has taught a processor, comprising:

a branch predictor to issue a first branch prediction at a branch point in a program *[Branch predictions are issued at a branch point in a program (page 110, 1ˢᵗ paragraph). The inherent mechanism that issues the branch predictions is a branch predictor]*;

a first circuit *[Dynamic Control Independence (DCI) Buffer; See Fig. 3]* to detect an exact convergence point subsequent to said branch point in said program, said exact convergence point being a point at which a path mispredicted from said branch point converges with a correct path at a point of said correct path immediately following said branch point *[The DCI Buffer detects the first control independent instruction subsequent to the branch location (page 111, 1ˢᵗ column, lines 6-9). An exact convergence point is a particular type of first control independent instruction and is, therefore, detected]*; and

a circuit to re-execute selected instructions *[instructions that are control independent]* of said program subsequent to said branch point, only upon detecting said exact convergence point *[page 110, 2ⁿᵈ column, 1ˢᵗ paragraph]*;

a second circuit *[WP Bit Mask; See Fig. 3]* to track a first set of physical registers written subsequent to said branch point *[The WP Bit Mask tracks the physical registers written subsequent to the branch point and prior to the first control independent instruction (e.g. exact convergence point) (page 111, section 2.1.2.1)]*.

Chou does not expressly disclose a scheduler to store instructions of the program subsequent to said branch point when said branch prediction is a misprediction and, further, that the scheduler re-executes the re-executed instructions.

Keller discloses a scheduler *[Keller; Fig. 1, component 36]* to store instructions of

the program subsequent to said branch point when said branch prediction is a

misprediction wherein the scheduler re-executes instructions subsequent to a branch

[Since a branch prediction allows instructions of a program subsequent to a branch

point to be available for execution and the scheduler stores instructions available for

execution (Keller; column 8, lines 7-27), the scheduler stores instructions of a program

subsequent to the branch point. This happens regardless of whether the prediction was

correct or incorrect (i.e. a misprediction)].

At the time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the processor of Chou to include a scheduler to store

instructions of the program subsequent to said branch point when said branch

prediction is a misprediction wherein the scheduler re-executes the re-executed

instructions as taught by Keller.

The suggestion/motivation for doing so would have been that doing so

advantageously maximizes the execution rate *[Keller; column 1, lines 39-47].*

8.   Referring to claim 3, Chou and Keller have taught the processor of claim 2,

wherein said selected instructions include a first set of instructions of said program

[instructions that are control independent and data independent] whose source physical

registers were tracked by said second circuit *[Chou; page 111, section 2.1.2.1].*

9.   Referring to claim 4, Chou and Keller have taught the processor of claim 2,

wherein said scheduler further executes move instructions corresponding to a second

set of instructions *[Chou; instructions that are control dependent]* that write to said first

set of physical registers prior to said exact convergence point *[Instructions that are control independent and data dependent are reexecuted. These instructions correspond to the instructions that are control dependent since the later instructions write to the registers that are the sources of the former instructions (page 111, section 2.1.2.1)].*

10.   Referring to claim 5, <u>Chou</u> and <u>Keller</u> have taught the processor of claim 2, further comprising a recovery buffer *(<u>Chou</u>; reorder buffer)* to store said selected instructions outside said scheduler *[All instructions, including the aforementioned control independent instructions, are stored in the reorder buffer upon dispatch. (<u>Chou</u>; page 110, 2nd column, 3rd paragraph)].*

11.   Referring to claim 8, <u>Chou</u> and <u>Keller</u> have taught the processor of claim 1, wherein said second circuit *(WP Bit Mask)* is a scoreboard including a set of flags corresponding to a set of physical registers *[The WP Bit Mask includes a bit (i.e. flag) for each physical register (page 111, column 1, last paragraph)]*, wherein one of said set of flags is set when a corresponding one of said set of physical registers is written between said branch point and said exact convergence point *[<u>Chou</u>; The WP Bit Mask indicates the physical registers written to by instructions on the wrong path (i.e. instructions between the branch point and the exact convergence point (page 111, column 1, last paragraph)].*

12.   Referring to claim 9, <u>Chou</u> and <u>Keller</u> have taught the processor of claim 8, wherein said one of said set of flags *(WP Bit Mask)* is cleared when said corresponding one of said set of physical registers is written subsequent to said exact convergence

point *[Chou; Data independent instructions subsequent to the first control independent instruction (e.g. exact convergence point) clear the bit (i.e. flag) corresponding to the physical register that is written to by the instruction (page 111, column 2, lines 7-12)].*

13.   Referring to claim 10, <u>Chou</u> has taught a method, comprising:

tracking a set of physical registers written by a first selected subset *[instructions that are control dependent]* of a set of instructions *[The WP Bit Mask tracks the physical registers written subsequent to the branch point and prior to the first control independent instruction (e.g. exact convergence point) (page 111, section 2.1.2.1)]*; and

re-executing a second selected subset *[Instructions that are control independent and data dependent]* of said set of instructions subsequent to an exact convergence point, that use a first one of said set of physical registers as a source operand register, only upon detecting said exact convergence point, said exact convergence point being a point at which a path mispredicted from said mispredicted branch point converges with a correct path at a point of said correct path immediately following said mispredicted branch point *[The DCI Buffer detects the first control independent instruction (e.g. an exact convergence point) subsequent to the branch location (page 111, 1ˢᵗ column, lines 6-9) and, only upon detecting the exact convergence point, re-executes instructions that are control independent and data dependent (page 110, 2ⁿᵈ column, 1ˢᵗ paragraph). The control independent and data dependent instructions are indicated by the use of one of said physical registers as a source operand (page 111, section 2.1.2.1)].*

<u>Chou</u> does not expressly disclose storing a set of instructions of a program subsequent to a mispredicted branch point.

Keller discloses a scheduler *[Keller; Fig. 1, component 36]* that stores a set of

instructions of a program subsequent to a mispredicted branch point *[Since a branch*

prediction allows instructions of a program subsequent to a branch point to be available

for execution and the scheduler stores instructions available for execution (Keller;

column 8, lines 7-27), the scheduler stores instructions of a program subsequent to the

branch point. This happens regardless of whether the prediction was correct or

incorrect (i.e. a misprediction)].

At the time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the processor of Chou to include stores a set of

instructions of a program subsequent to a mispredicted branch point as taught by Keller.

The suggestion/motivation for doing so would have been that doing so

advantageously maximizes the execution rate *[Keller; column 1, lines 39-47].*

14.   Referring to claim 11, Chou and Keller have taught the method of claim 10,

wherein said tracking includes setting a flag for a second one of said set of physical

registers written on a mispredicted path subsequent to said mispredicted branch point

[Chou; The WP Bit Mask is set to indicate the physical registers written to by

instructions on the wrong path (i.e. instructions between the branch point and the exact

convergence point (page 111, column 1, last paragraph)].

15.   Referring to claim 12, Chou and Keller have taught the method of claim 11,

further comprising clearing said flag when an instruction subsequent to said exact

convergence point uses said second one of said set of physical registers as a source

register *[Chou; Data independent instructions subsequent to the first control*

independent instruction (e.g. exact convergence point) clear the bit (i.e. flag)

corresponding to the physical register that is written to by the instruction (page 111,

column 2, lines 7-12)].

16.   Referring to claim 13, <u>Chou</u> and <u>Keller</u> have taught the method of claim 10,

wherein said storing includes placing said set of instructions in a restore buffer *(Chou;*

reorder buffer) prior to reloading them into a scheduler *[All instructions are stored in the*

reorder buffer upon dispatch. (Chou; page 110, 2nd column, 3rd paragraph)].

17.   Referring to claim 14, <u>Chou</u> and <u>Keller</u> have taught the method of claim 10,

wherein said restoring includes executing a corresponding move instruction for each of

said first selected subset of said set of instructions *[Chou; Instructions that are control*

independent and data dependent are reexecuted. These instructions correspond to the

instructions that are control dependent (i.e. the first selected subset) since the later

instructions write to the registers that are the sources of the former instructions (page

111, section 2.1.2.1)].

18.   Referring to claim 16, <u>Chou</u> has taught a system, comprising:

        a processor including

                a branch predictor to issue a first branch prediction at a branch point in a

        program *[Branch predictions are issued at a branch location in a program (page*

        110, 1st paragraph). The inherent mechanism that issues the branch predictions

        is a branch predictor];

                a first circuit *[Dynamic Control Independence (DCI) Buffer; See Fig. 3]* to

        detect an exact convergence point subsequent to said branch point in said

program, said exact convergence point being a point at which a path

mispredicted from said branch point converges with a correct path at a point of

said correct path immediately following said branch point *[The DCI Buffer detects*

the first control independent instruction subsequent to the branch location (page

111, 1st column, lines 6-9). An exact convergence point is a particular type of

first control independent instruction and is, therefore, detected]; and

a circuit to re-execute selected instructions *[instructions that are control*

independent] of said program subsequent to said branch point, only upon

detecting said exact convergence point *[The DCI Buffer detects an exact*

convergence point subsequent to the branch location and, only upon detecting

the exact convergence point, re-executes instructions that are control

independent (page 110, 2nd column, 1st paragraph)]

a second circuit *[WP Bit Mask; See Fig. 3]* to track a first set of physical

registers written subsequent to said branch point *[The WP Bit Mask tracks the*

physical registers written subsequent to the branch point and prior to the first

control independent instruction (e.g. exact convergence point) (page 111, section

2.1.2.1)].

Chou does not expressly disclose a scheduler to store instructions of the

program subsequent to said branch point when said branch prediction is a misprediction

and, further, that the scheduler re-executes the re-executed instructions.

Keller discloses a scheduler *[Keller; Fig. 1, component 36]* to store instructions of

the program subsequent to said branch point when said branch prediction is a

misprediction wherein the scheduler re-executes instructions subsequent to a branch

[Since a branch prediction allows instructions of a program subsequent to a branch

point to be available for execution and the scheduler stores instructions available for

execution (Keller; column 8, lines 7-27), the scheduler stores instructions of a program

subsequent to the branch point. This happens regardless of whether the prediction was

correct or incorrect (i.e. a misprediction)].

At the time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the processor of <u>Chou</u> to include a scheduler to store

instructions of the program subsequent to said branch point when said branch

prediction is a misprediction wherein the scheduler re-executes the re-executed

instructions as taught by <u>Keller</u>.

The suggestion/motivation for doing so would have been that doing so

advantageously maximizes the execution rate *[Keller; column 1, lines 39-47].*

<u>Chou</u> and <u>Keller</u> do not expressely disclose an interface to couple the processor

to input-output devices and an audio input-output device coupled to said interface to

receive audio data from said processor.

However, Examiner takes Official Notice that an interface to couple a processor

to input-output devices and an audio input-output device coupled to the interface to

receive audio data from the processor is a conventional and well-known means

communicating input-output data.

It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the system of <u>Chou</u> and <u>Keller</u> to include an interface to

couple a processor to input-output devices and an audio input-output device coupled to

the interface since doing so would advantageously allow the processor to communicate

information with a user in an audible manner.

19.   Referring to claim 17, given the similarities between claim 2 and claim 17 the

arguments as stated for the rejection of claim 2 also apply to claim 17.

20.   Referring to claim 18, given the similarities between claim 3 and claim 18 the

arguments as stated for the rejection of claim 3 also apply to claim 18.

21.   Referring to claim 19, given the similarities between claim 4 and claim 19 the

arguments as stated for the rejection of claim 4 also apply to claim 19.

22.   Referring to claim 20, given the similarities between claim 5 and claim 20 the

arguments as stated for the rejection of claim 5 also apply to claim 20.

23.   Referring to claim 23, given the similarities between claim 8 and claim 23 the

arguments as stated for the rejection of claim 8 also apply to claim 23.

24.   Referring to claim 24, given the similarities between claim 9 and claim 24 the

arguments as stated for the rejection of claim 9 also apply to claim 24.

25.   Referring to claim 25, given the similarities between claim 10 and claim 25 the

arguments as stated for the rejection of claim 10 also apply to claim 25.

26.   Referring to claim 26, given the similarities between claim 11 and claim 26 the

arguments as stated for the rejection of claim 11 also apply to claim 26.

27.   Referring to claim 27, given the similarities between claim 12 and claim 27 the

arguments as stated for the rejection of claim 12 also apply to claim 27.

28.   Referring to claim 28, given the similarities between claim 13 and claim 28 the

arguments as stated for the rejection of claim 13 also apply to claim 28.

29.   Referring to claim 29, given the similarities between claim 14 and claim 29 the

arguments as stated for the rejection of claim 14 also apply to claim 29.

30.   Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chou in view of Keller as applied to claim 1 above, and further in view of Hennessy et

al., "Computer Architecture: A Quantitative Approach", (Herein referred to as

Hennessy).

31.   Referring to claim 6, Chou and Keller have taught the processor of claim 1,

wherein said first circuit includes an alternate target buffer *[DCI Buffer]* coupled to said

branch target buffer for determining said exact convergence point *[The DCI Buffer is*

used to determine the first control independent instruction (e.g. exact convergence

point) (Chou; page 110, 4th paragraph, which continues on page 111)].

Chou and Keller have not explicitly taught that the branch predictor includes a

branch target buffer to store target addresses indexed by branch locations in said

program.

Hennessy has taught a branch predictor including a branch target buffer *[See*

Fig. 3.19] to store target addresses indexed by branch locations in said program

[Hennessy; page 209-210].

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the branch predictor of Chou and Keller to include a branch target buffer as taught by Hennessy.

The suggestion/motivation for doing so would have been that doing so reduces the branch penalty and allows a high-bandwidth instruction stream *[Hennessy; page 209, 3rd and 4th paragraphs]*.

32.   Referring to claim 21, given the similarities between claim 6 and claim 21 the arguments as stated for the rejection of claim 6 also apply to claim 21.

33.   Claims 7 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou in view of Keller in view of Hennessy as applied to claim 6 above, and further in view of Manne et al., "Branch prediction using selective branch inversion", (Herein referred to as Manne).

34.   Referring to claim 7, Chou, Keller, and Hennessy have taught the processor of claim 6.

Chou, Keller, and Hennessy have not explicitly taught that the branch predictor includes a branch confidence estimator to reverse a second branch prediction of low confidence to induce an induced exact convergence point.

Manne has taught a branch predictor includes a branch confidence estimator *[Manne; See Fig. 1]* to reverse (*i.e. invert*) a second branch prediction of low confidence *[Manne; Section 2.2, 3rd paragraph]* to induce an induced exact convergence point

[When a low confidence branch is predicted correctly and the prediction is inverted by the confidence estimator, the branch will be predicted incorrectly. In doing so, the confidence estimator will induce an induced exact convergence point (Manne; Section 2.2, 3rd paragraph)].

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the branch predictor of <u>Chou</u>, <u>Keller</u>, and <u>Hennessy</u> to include a branch confidence estimator as taught by <u>Manne</u>.

The suggestion/motivation for doing so would have been that doing so improves branch prediction in an efficient manner *[Manne; 3rd paragraph of introduction]*.

35.   Referring to claim 22, given the similarities between claim 7 and claim 22 the arguments as stated for the rejection of claim 7 also apply to claim 22.

36.   Claims 15 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Chou</u> in view of <u>Keller</u> as applied to claim 10 above, and further in view of <u>Manne</u>.

37.   Referring to claim 15, <u>Chou</u> and <u>Keller</u> have taught the method of claim 10.

<u>Chou</u> and <u>Keller</u> have not explicitly taught reversing a branch prediction of a subsequent branch point to induce said exact convergence point.

<u>Manne</u> has taught reversing a branch prediction of a subsequent branch point to induce said exact convergence point. *[When a low confidence branch is predicted the correctly and the prediction is inverted by the confidence estimator, the branch will be*

predicted incorrectly. In doing so, the confidence estimator will induce the exact

convergence point (Manne; Section 2.2, 3rd paragraph)].

At the time the invention was made, it would have been obvious to a person of

ordinary skill in the art to modify the branch predictor of Chou and Keller to include a

branch confidence estimator as taught by Manne.

The suggestion/motivation for doing so would have been that doing so improves

branch prediction in an efficient manner *[Manne; 3rd paragraph of introduction]*.

38.   Referring to claim 30, given the similarities between claim 15 and claim 30 the

arguments as stated for the rejection of claim 15 also apply to claim 30.

Response to Arguments

39.   Applicant's arguments filed 04/09/2007 have been fully considered but they are

not persuasive.

40.   Applicant argues the novelty/rejection of claims 1, 3-16, and 18-30 on pages 9-13

of the remarks, in substance that:

> "Hence, Chou re-executes instructions upon detecting a convergence point, regardless of
> whether it is an exact convergence point, see, e.g., Chou, at § 2.1.2.1, and thus does not re-
> execute instructions 'only upon detecting said exact convergence point,' as recited in claims 1
> and 16" (3rd paragraph on page 10)

These arguments are not found persuasive for the following reasons:

In response to the applicant's argument regarding the detecting an "exact

convergence point", the examiner first acknowledges the applicant's amendment to the

claims to explicitly define an "exact convergence point". As noted by the examiner and

recognized by the applicant in the remarks, Chou detects all convergence points (which

are referred to in Chou as first control independent instructions) and, therefore, Chou

detects "exact convergence points" as defined by the claims.

Regarding the applicant's argument that Chou has not taught re-executing

instructions only upon detecting said exact convergence point, the examiner notes that,

in the context of an instruction sequence containing an exact convergence point, Chou

re-executes selected instructions only upon detecting the exact convergence point (1st

paragraph of section 2.1). That is, in the context of an instruction sequence containing

an exact convergence point, Chou and the applicant's claimed invention operate in the

same manner. Therefore, Chou has taught the invention as claimed. It appears to the

examiner that the applicant's amendment regarding re-executing "only upon detecting

said exact convergence point" is intended to differentiate between what happens in the

system of Chou and the applicant's system (as disclosed in the specification) when a

regular convergence point is detected since the claimed invention and Chou function in

the same manner in the context of an exact convergence point. If such is the case, the

examiner suggests that the applicant amend the claims to indicate the operation of the

system in the presence of a regular convergence point.

Conclusion

41.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

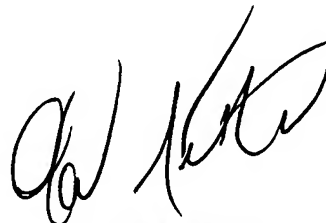MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER